**AMENDMENTS TO THE CLAIMS**

**(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)**

Please cancel claims 6 and 7 without prejudice.

1. (CURRENTLY AMENDED) A method for synchronizing a clock signal to a data signal, comprising the steps of:

(A) detecting an edge of said data signal;

(B) generating a ~~numeric representation of a~~ relative polarity and a magnitude of a phase error between (i) said edge of said data signal and (ii) said clock signal;

(C) determining whether said ~~numeric representation~~ magnitude is within a predetermined zone;

(D) ~~if said numeric representation is not within said predetermined zone, adjusting said clock signal towards said position of said edge; and~~

~~(E)~~ if said ~~numeric representation~~ magnitude is within said predetermined zone, repeating steps (A)-(C);

(E) if said magnitude is not within said predetermined zone, determining whether said relative polarity is a positive polarity or a negative polarity;

(F) if said relative polarity is positive, incrementing an accumulated value to adjust said position of said edge; and

(G) if said relative polarity is negative, decrementing said accumulated value to adjust said position of said edge.

2. (ORIGINAL) The method of claim 1, wherein step (A) comprises the sub-step of:

(A-1) sampling a number of clock signals using said data signal.

3. (ORIGINAL) The method according to claim 2, wherein step (A) further comprises the sub-step of:

(A-2) encoding a position of said edge.

4. (ORIGINAL) The method of claim 1, wherein step (B) further comprises:

comparing an encoded position of said edge to a predetermined value.

5. (ORIGINAL) The method of claim 3, wherein step (A) further comprises the sub-step of:

storing said encoded position.

6. (CANCELED)

7. (CANCELED)

8. (PREVIOUSLY PRESENTED) The method of claim 1, wherein step (C) further comprises the sub-step of selecting a number of clock phases based upon said accumulated value.

9. (CURRENTLY AMENDED) An apparatus for synchronizing a clock signal to a data signal, comprising:

a detector configured to produce a ~~numeric value~~ relative polarity and a magnitude representing a position of an edge of said data signal based upon a state of said clock signal; and

a control circuit configured to adjust said clock signal ~~when said position of said edge is not within a predetermined zone, wherein said adjustment comprises adjusting said clock signal towards said position of said edge~~ by determining whether said magnitude is within a predetermined zone, and if said magnitude is not within said predetermined zone, determining whether said relative polarity is a positive polarity or a negative polarity and (i) if said relative polarity is positive, incrementing an accumulated value to adjust said position of said edge, and (ii) if said relative polarity is negative, decrementing said accumulated value to adjust said position of said edge.

10. (CURRENTLY AMENDED) The apparatus of claim 9, wherein ~~the~~ said control ~~circuitry~~ circuit further comprises a storage element configured to store an accumulated value representing an encoded position of said edge.

11. (CURRENTLY AMENDED) The apparatus of claim 9, wherein said control ~~circuitry~~ circuit further comprises an increment/decrement logic circuit configured to adjust said accumulated value in response to said relative polarity and

magnitude ~~numeric value~~, wherein said ~~accumulated value is~~ relative polarity and magnitude are updated each time said detector produces said relative polarity and magnitude ~~numeric value~~.

12. (ORIGINAL) The apparatus of claim 9, wherein said clock signal comprises a plurality of phases.

13. (CURRENTLY AMENDED) The apparatus of claim ~~9~~12, wherein said control ~~circuitry~~ circuit selects one or said plurality of phases as a system clock.

14. (CURRENTLY AMENDED) An apparatus for synchronizing a clock signal to a data signal, comprising:

means for detecting an edge of said data signal;

means for generating a ~~numeric representation of a~~ relative polarity and a magnitude of a phase error between (i) said edge of said data signal and (ii) said clock signal;

means for determining whether said ~~numeric representation~~ magnitude is within a predetermined zone; and

means for ~~adjusting~~ determining whether said relative polarity is a positive polarity or a negative polarity and (i) if said relative polarity is positive, incrementing an accumulated value to adjust said position of said edge, and (ii) if said relative polarity is negative, decrementing said accumulated value to adjust said position of said edge ~~said clock signal towards said~~

~~position of said edge when said position of said edge is not within said predetermined zone; and~~

~~if said numeric representation is within said predetermined zone, repeating steps (A)-(D)~~.

15. (CURRENTLY AMENDED) A method for synchronizing a clock signal to a data signal, comprising the steps of:

(A) detecting an edge of a data signal;

(B) determining a relative polarity and a phase offset magnitude as a numeric representation of said edge of said data signal relative to said clock signal;

(C) if said phase offset magnitude is less than a predetermined value, repeating steps (A) and (B);

(D) if said magnitude is greater than a predetermined value, determining a polarity of said phase offset magnitude~~.~~; and

(E) adjusting said clock signal (i) counter-clockwise if said polarity is positive and (ii) clockwise if said polarity is not positive.

16. (PREVIOUSLY PRESENTED) The method according to claim 15, further comprising the step of:

generating an accumulated value for said numeric representation of said magnitude, wherein said accumulated value is updated each pass through step (B).